

In the Claims

1. (Currently Amended) A method for fabricating a semiconductor device comprising:  
forming a gate oxide and a gate electrode on a semiconductor substrate;  
performing a first ion implantation process for the formation of a (lightly doped drain) LDD region in the substrate;  
forming spacers on the sidewalls of the gate electrode;  
performing a second ion implantation process for the formation of a junction region in the substrate using the spacers as a mask;  
forming a trench for device isolation by removing selectively the top portion of the substrate between the spacers;  
forming an ~~oxidation~~ oxide layer on the whole substrate except on the spacers;  
forming a diffusion barrier on the resulting substrate;  
depositing a gap filling insulation layer over the diffusion barrier;  
planarizing the gap filling insulating layer; and  
removing selectively some part of the gap filling insulation layer to form contact holes.
2. (Original) A method as defined by claim 1, wherein the gap filling insulation layer is formed of boro-phosphosilicate glass (BPSG).
3. (Original) A method as defined by claim 1, wherein the diffusion barrier is formed of amorphous silicon.
4. (Original) A method as defined by claim 1, wherein the diffusion barrier is an N-doped oxide layer.
5. (Original) A method as defined by claim 1, wherein the gap filling insulation layer is formed of undoped silicate glass (USG).
6. (Original) A method as defined by claim 1, wherein the gap filling insulation layer is used as both a device isolation layer and an interlayer insulation layer.